



Q77H2-AD

Rev : A

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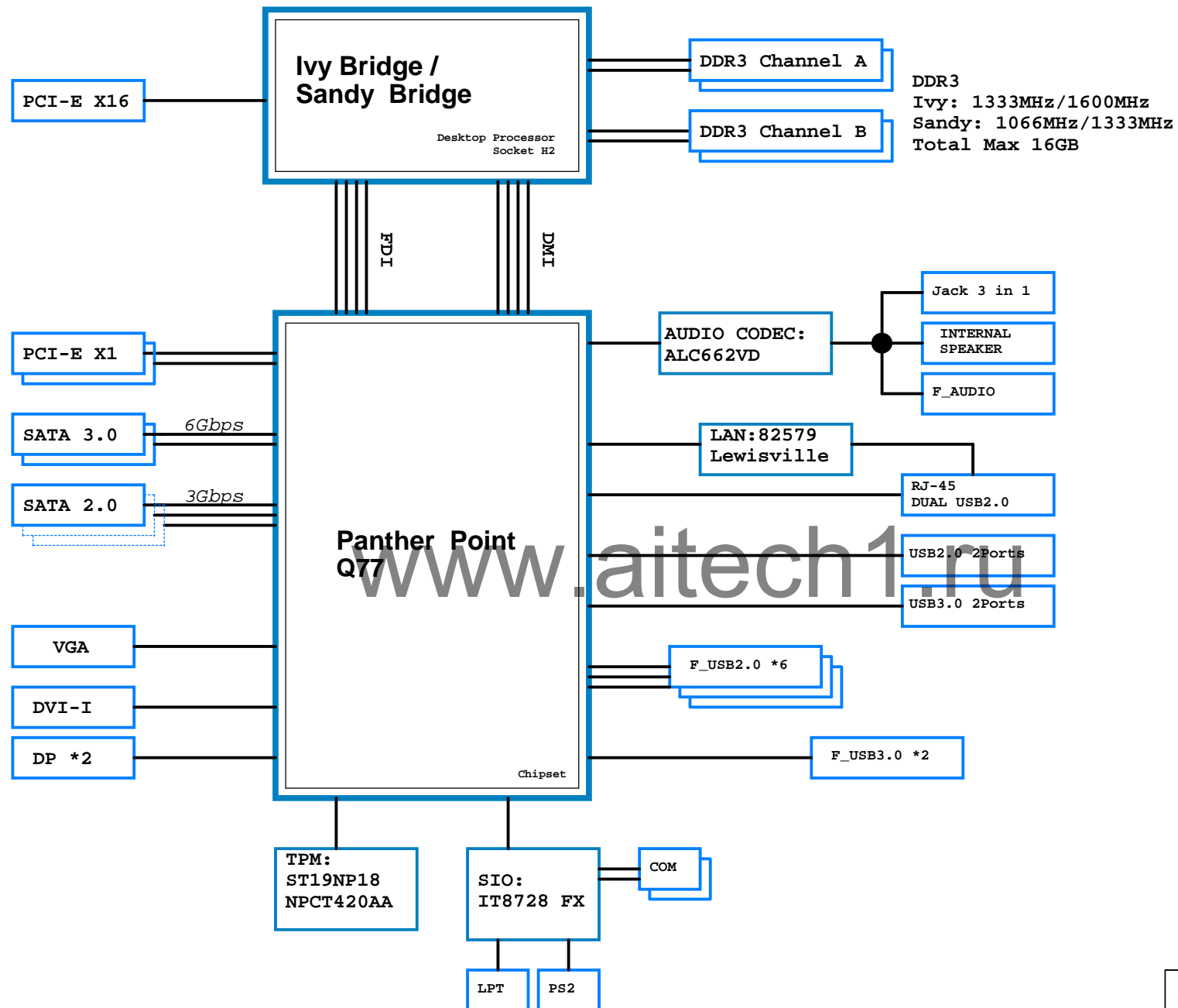
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REVISION HISTORY:

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Rev	Date	Notes
V.A	2011/10/03	Initial version

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GPIO Table

PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4SS

IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

Strapping Table

PCH Strapping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

SIO IT8728F D/EX Strapping (Page.28)

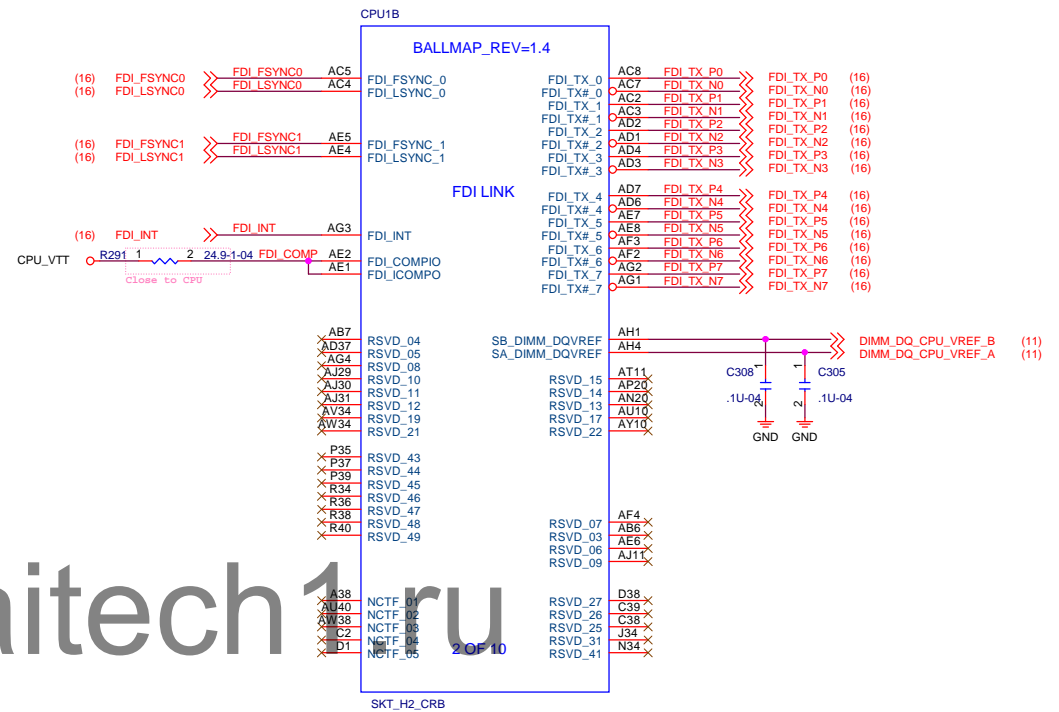
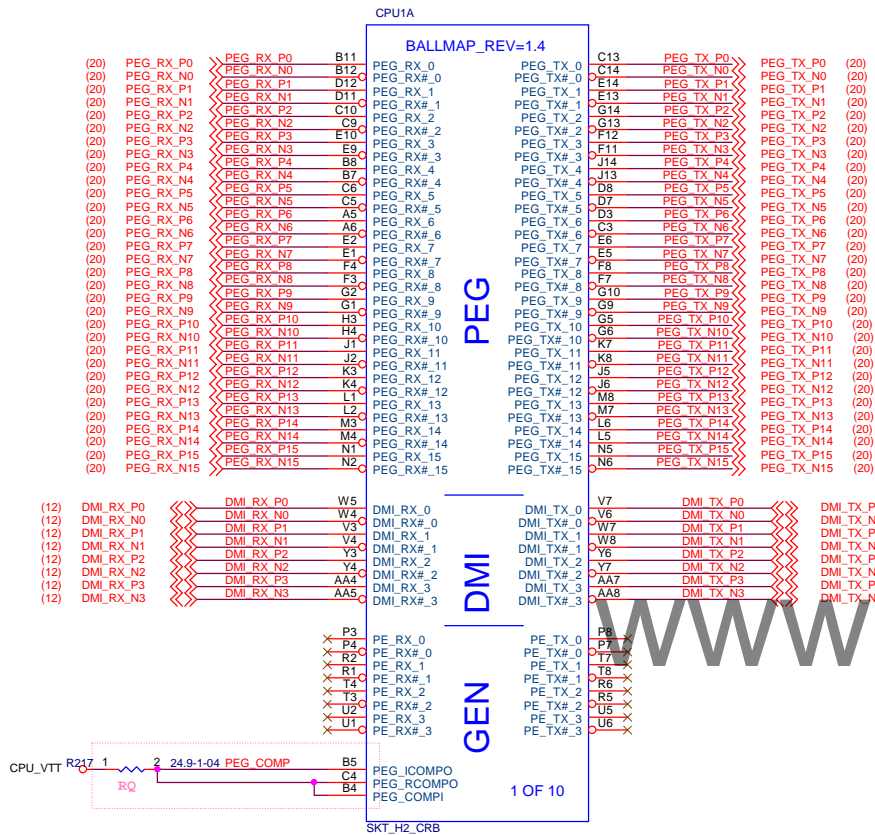
Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-48		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-29	OV/UV	0	Force Mode

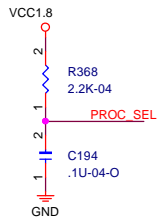


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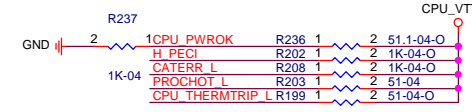
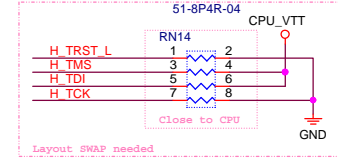
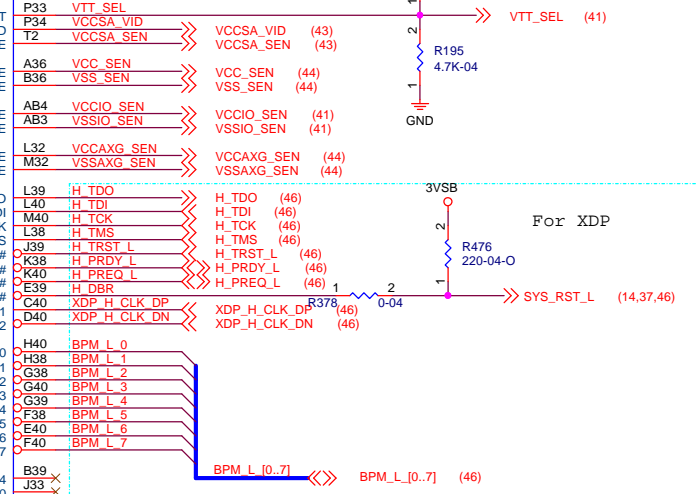
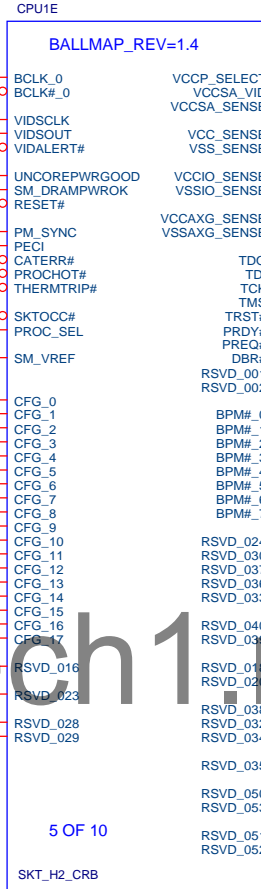
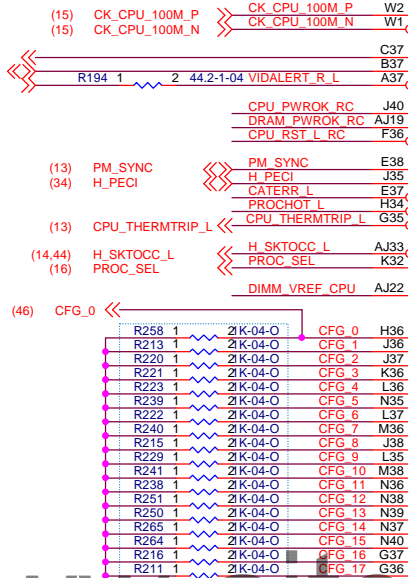
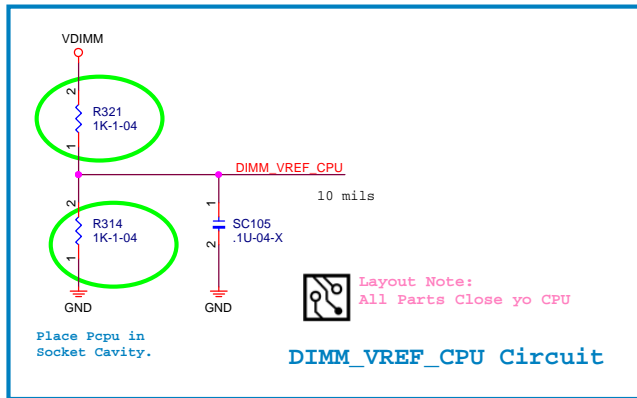
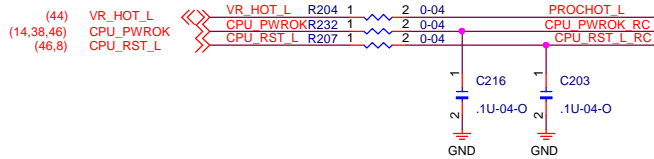
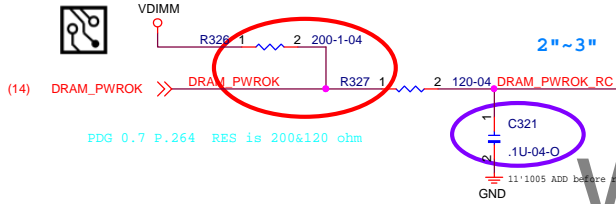
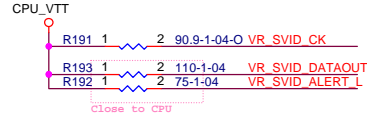
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GPIO Function Map		
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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC 1SP SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	+	+	PEOFGSEL[0]
6	+	+	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SELO	SEL1
1X16	1	1
2X8	0	1

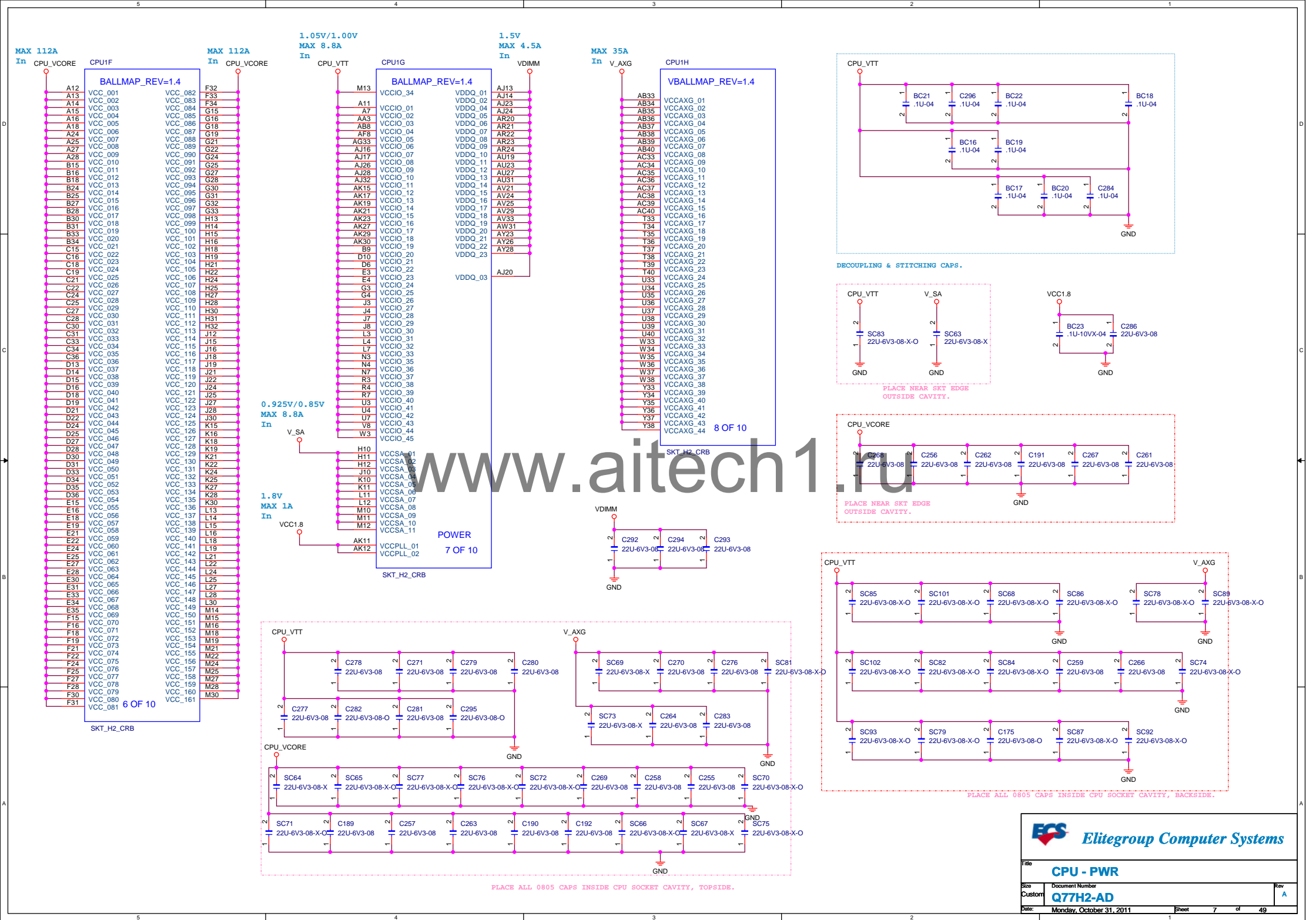
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CPU - MISC

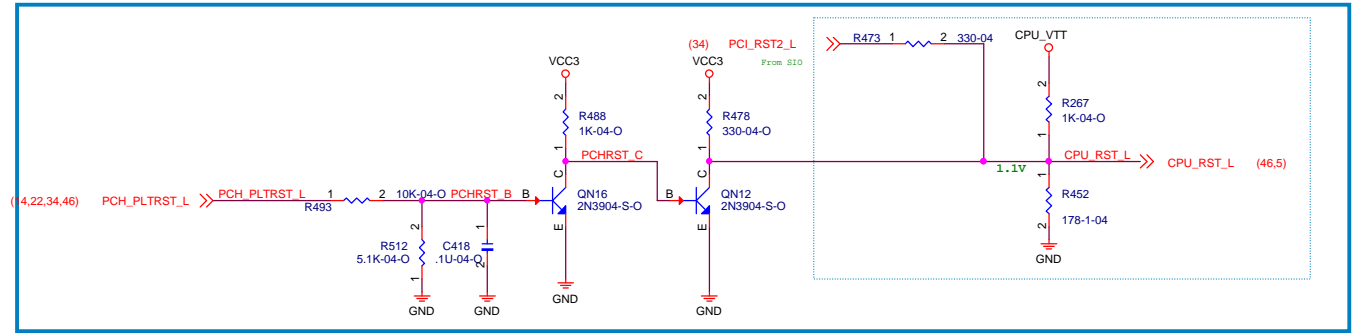
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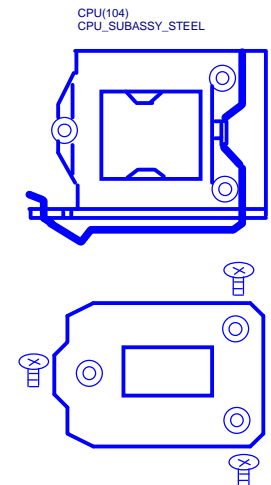
CPU1I			CPU1J		
BALLMAP_REV=1.4			BALLMAP_REV=1.4		
A17	VSS_001	AM27	AV11	VSS_181	G8
A23	VSS_002	AM3	AV14	VSS_182	H1
A26	VSS_003	AM30	AV17	VSS_183	H17
A29	VSS_004	AM36	AV3	VSS_184	H2
AA35	VSS_005	AM37	AV35	VSS_185	H20
AA33	VSS_006	AM38	AV38	VSS_186	H23
AA34	VSS_007	AM39	AV6	VSS_187	H26
AA35	VSS_008	AM40	AW10	VSS_188	H29
AA36	VSS_009	AM5	AW11	VSS_189	H33
AA37	VSS_010	AN10	AW14	VSS_190	H37
AA38	VSS_011	AN11	AW16	VSS_191	H39
AA6	VSS_012	AN17	AW36	VSS_192	H5
AB5	VSS_013	AN22	AW6	VSS_193	H6
AC1	VSS_014	AN27	AY4	VSS_194	H9
AC6	VSS_015	AN30	AY6	VSS_195	J11
AD33	VSS_016	AN31	AY8	VSS_196	J17
AD36	VSS_017	AN32	B10	VSS_197	J20
AD38	VSS_018	AN33	B13	VSS_198	J23
AD39	VSS_019	AN34	B17	VSS_199	J26
AD40	VSS_020	AN35	B23	VSS_200	J29
AD5	VSS_021	AN36	B26	VSS_201	J32
AD8	VSS_022	AN5	B29	VSS_202	K1
AE3	VSS_023	AN6	B35	VSS_203	K12
AE33	VSS_024	AN7	B38	VSS_204	K13
AE36	VSS_025	AN8	B6	VSS_205	K14
AF1	VSS_026	AN9	C11	VSS_206	K17
AF6	VSS_027	AP1	C12	VSS_207	K2
AF7	VSS_028	AP11	C17	VSS_208	K20
AF37	VSS_029	AP17	C20	VSS_209	K23
AF40	VSS_030	AP22	C23	VSS_210	K26
AF5	VSS_031	AP25	C26	VSS_211	K29
AF6	VSS_032	AP27	C29	VSS_212	K33
AF7	VSS_033	AP30	C32	VSS_213	K35
AG36	VSS_034	AP37	C35	VSS_214	K37
AH2	VSS_035	AP4	C7	VSS_215	K39
AH3	VSS_036	AP40	C8	VSS_216	K5
AH33	VSS_037	AP5	D17	VSS_217	K6
AH36	VSS_038	AP5	D2	VSS_218	L10
AH37	VSS_039	AR11	D22	VSS_219	L17
AH38	VSS_040	AR14	D23	VSS_220	L20
AH39	VSS_041	AR18	D26	VSS_221	L23
AH40	VSS_042	AR19	D29	VSS_222	L26
AH5	VSS_043	AR27	D32	VSS_223	L29
AH8	VSS_044	AR30	D37	VSS_224	L34
AJ12	VSS_045	AR36	D39	VSS_225	M1
AJ15	VSS_046	AR5	D4	VSS_226	M17
AJ18	VSS_047	AT1	D5	VSS_227	M2
AJ21	VSS_048	AT10	D9	VSS_228	M20
AJ25	VSS_049	AT12	E11	VSS_229	M23
AJ5	VSS_050	AT13	E12	VSS_230	M29
AJ36	VSS_051	AT15	E17	VSS_231	M33
AK1	VSS_052	AT16	E20	VSS_232	M35
AK10	VSS_053	AT17	E23	VSS_233	M37
AK13	VSS_054	AT2	E26	VSS_234	M39
AK14	VSS_055	AT25	E29	VSS_235	M5
AK16	VSS_056	AT27	E32	VSS_236	M6
AK22	VSS_057	AT28	E36	VSS_237	M9
AK28	VSS_058	AT29	F1	VSS_238	N8
AK31	VSS_059	AT3	F10	VSS_239	P1
AK32	VSS_060	AT30	F14	VSS_240	P2
AK33	VSS_061	AT31	F17	VSS_241	P36
AK34	VSS_062	AT32	F2	VSS_242	P38
AK35	VSS_063	AT33	F20	VSS_243	P40
AK36	VSS_064	AT34	F23	VSS_244	P5
AK37	VSS_065	AT35	F26	VSS_245	P6
AK4	VSS_066	AT36	F29	VSS_246	P37
AK40	VSS_067	AT37	F35	VSS_247	R39
AK5	VSS_068	AT38	F37	VSS_248	R8
AK6	VSS_069	AT39	F39	VSS_249	T1
AK7	VSS_070	AT4	F4	VSS_250	T5
AK8	VSS_071	AT40	F5	VSS_251	T6
AK9	VSS_072	AT4	F6	VSS_252	T8
AL11	VSS_073	AT4	F9	VSS_253	U8
AL14	VSS_074	AT4	G11	VSS_254	V1
AL17	VSS_075	AT4	G12	VSS_255	V2
AL19	VSS_076	AT4	G17	VSS_256	V3
AL24	VSS_077	AT4	G20	VSS_257	V34
AL27	VSS_078	AT4	G23	VSS_258	V35
AL30	VSS_079	AT4	G26	VSS_259	V36
AL36	VSS_080	AT4	G29	VSS_260	V37
AL5	VSS_081	AT4	G34	VSS_261	V38
AM1	VSS_082	AT4	G7	VSS_262	V39
AM11	VSS_083	AT4	AY37	VSS_263	V40
AM14	VSS_084	AT4	B3	VSS_264	V5
AM17	VSS_085	AT4	VSS_NCTF_03	VSS_265	W6
AM2	VSS_086	AT4	VSS_NCTF_04	VSS_266	Y8
AM21	VSS_087	AT4		VSS_267	
AM23	VSS_088	AT4		VSS_268	
AM25	VSS_089	AT4		VSS_269	
	VSS_090	AT4		VSS_270	
A4	VSS_NCTF_01				
AV39	VSS_NCTF_02				

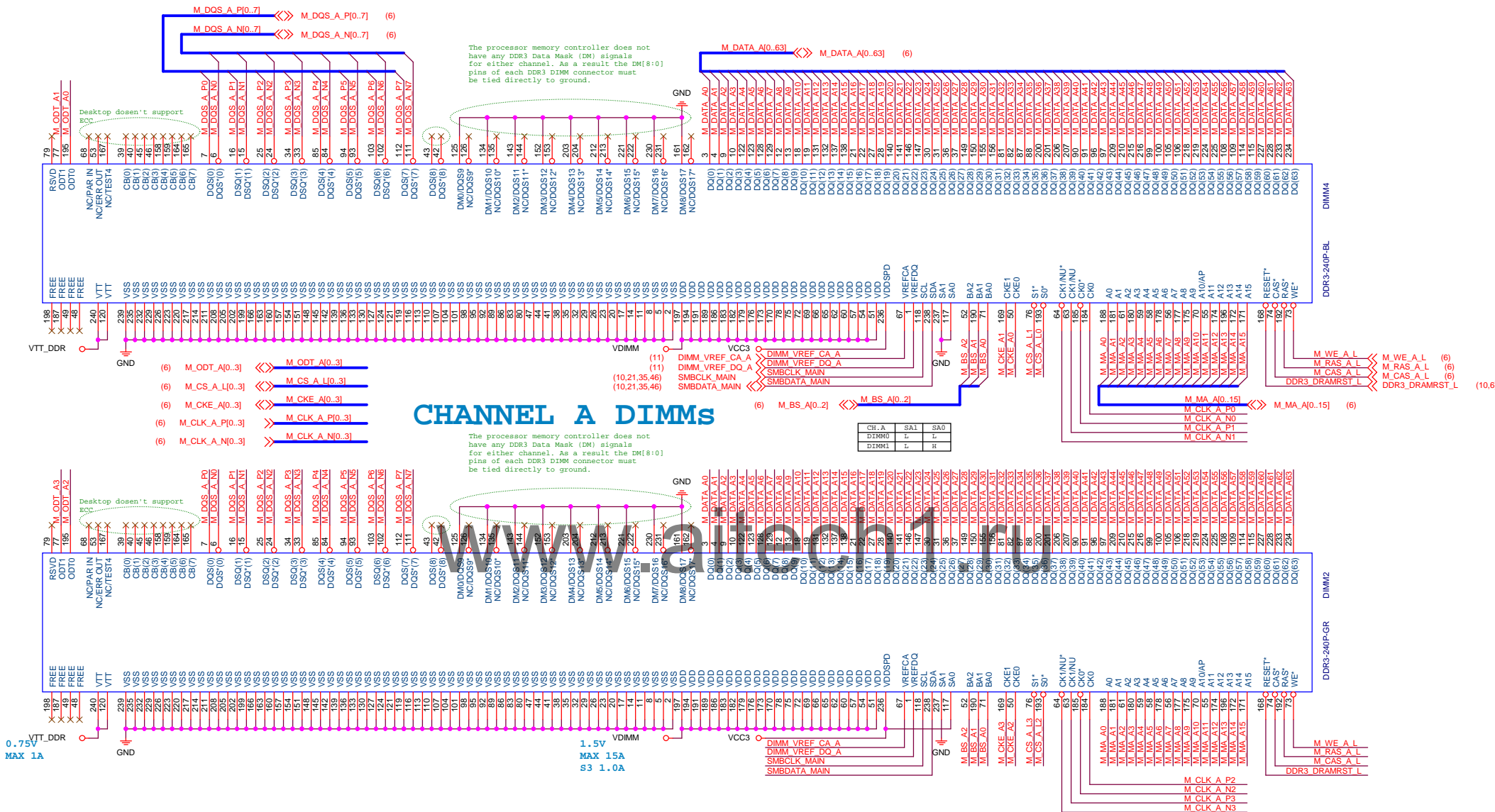


PLTRST_L Driving Circuit

11-018-115123 CPU GND SOCKET
SOCKET.CPU.LGA 1155P SMD..G/F...BLACK.
ACA-ZIF-096-B02...LEAD-FREE(RoHS/HP).L0TES

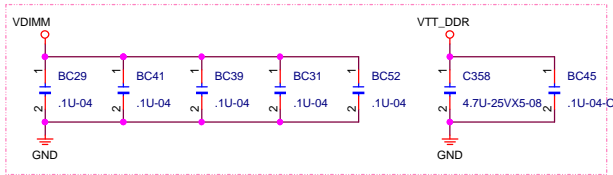
20-800-005011 SUBASSY.STEEL...LGA 1155P...
W/BACK PLATE.ACA-ZIF-082-E23...LEAD-FREE(RoHS/HP).L0TES



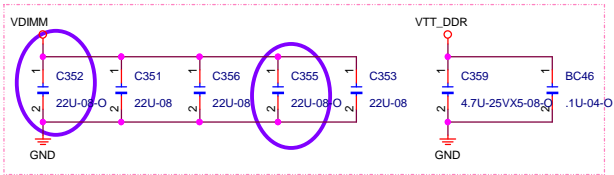


CHANNEL A DIMMS

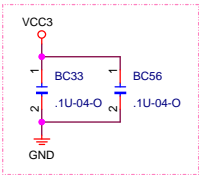
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



For CHAD1



For CHAD2



PLACE BETWEEN CHA & CHB.
DO NOT PUNCH VIA.

File

DDR3 - CHA DIMM0/1

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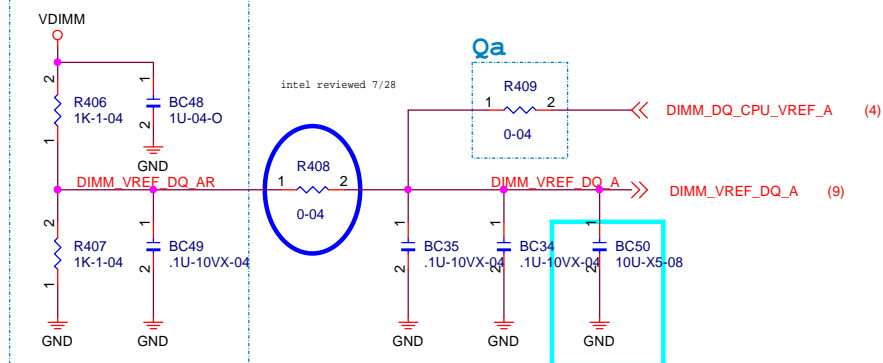
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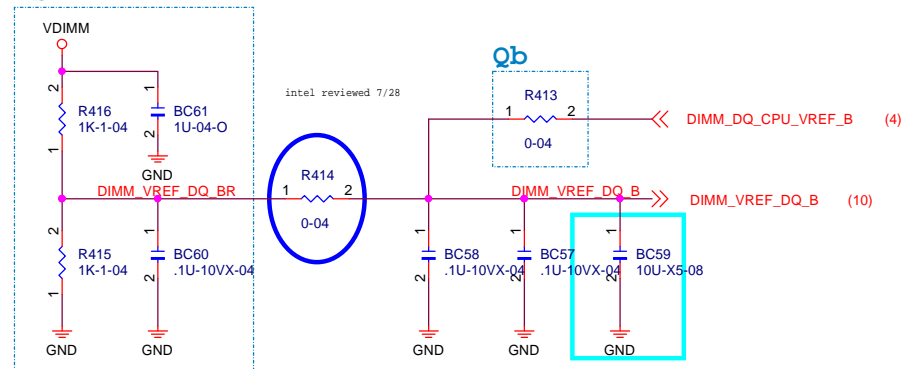
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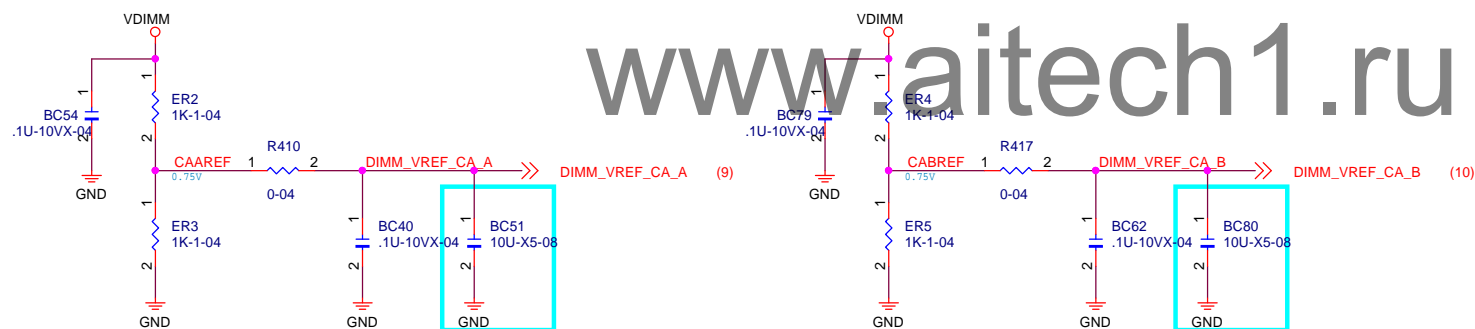
Layout Note:
All parts close to DDR3 Slots.

Pb



DIMM_VREF_DQ Control Circuit

www.aitech1.ru



DIMM_VREF_CA Circuit



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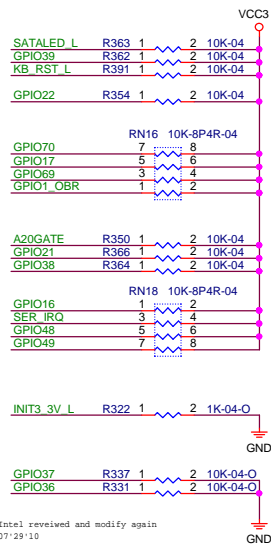
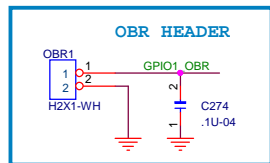
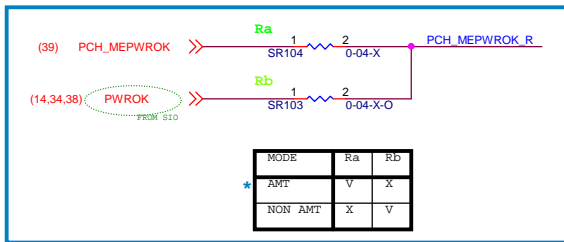
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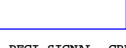
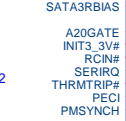
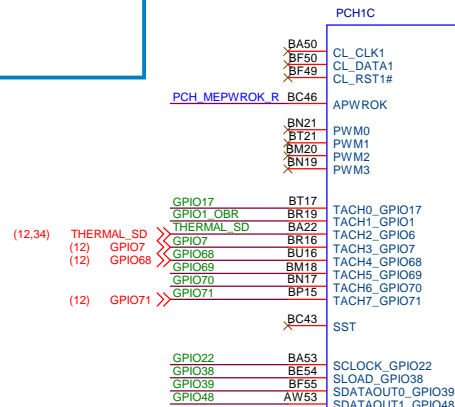
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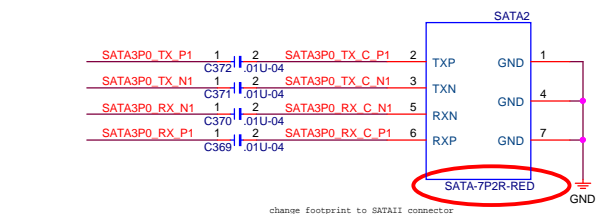
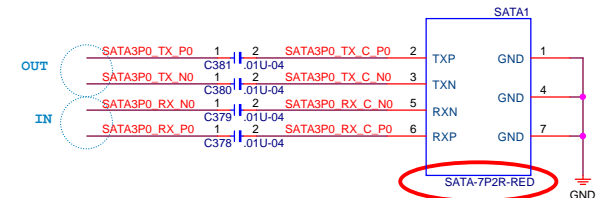
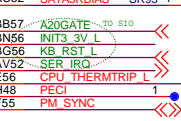
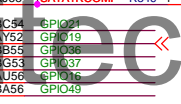
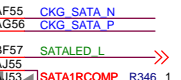
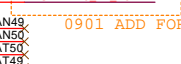
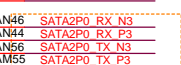
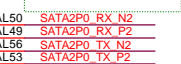
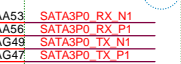
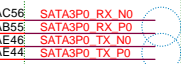
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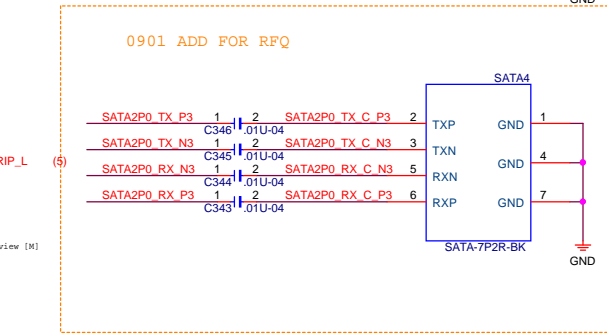
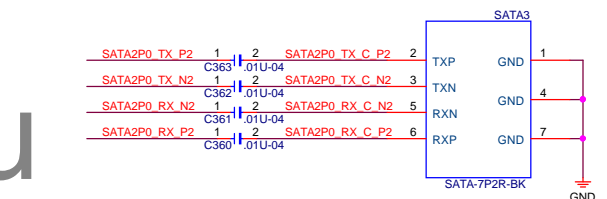
Intel received and modify again
07/29/10



PECI SIGNAL, CRB RESERVE CONNECT FROM CPU



Layout Note:
SATA3.0 4.5/7.5/20 in 90 Q ±17.5%
SATA2.0 4.5/7.5/15 in 90 Q ±17.5%

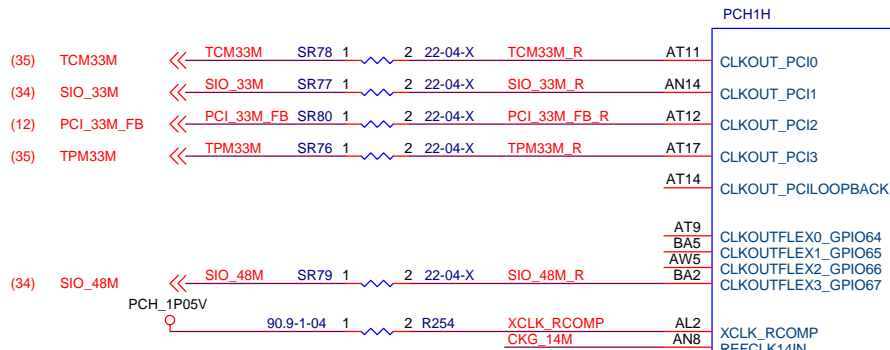


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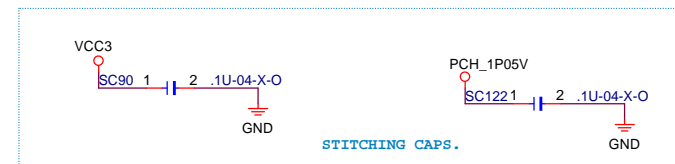
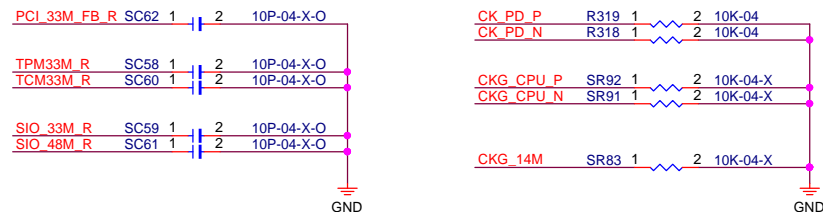
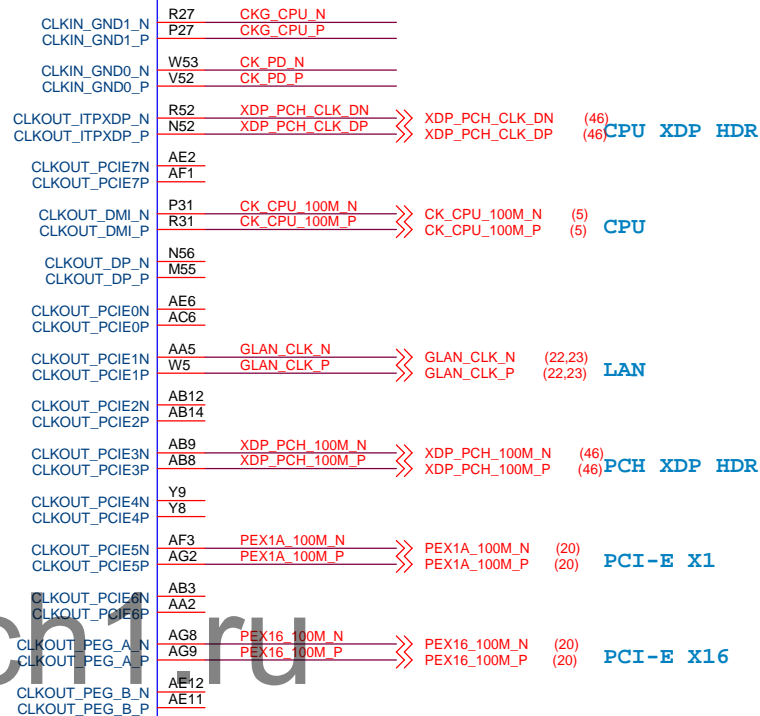
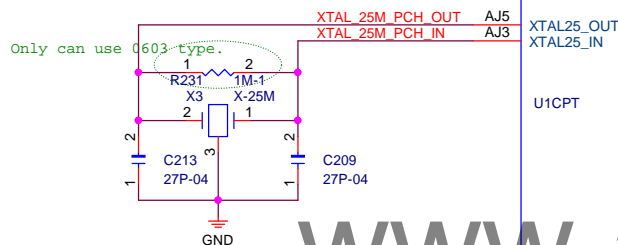
Title: **PCH - SATA, SATA CONN, OBR**

Size: Custom Document Number: **Q77H2-AD** Rev: **A**

Date: **Monday, October 31, 2011** Sheet: **13** of **49**



Layout Note:
PCI Clock Max 15000MILS



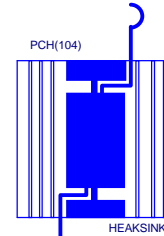
Elitegroup Computer Systems

Title: **PCH - CLK IO**

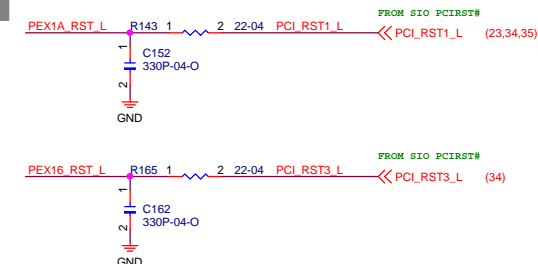
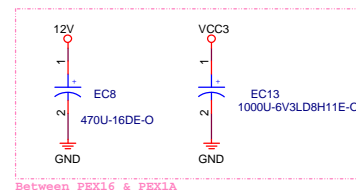
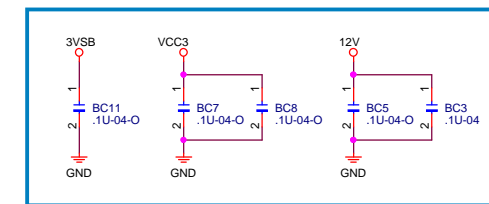
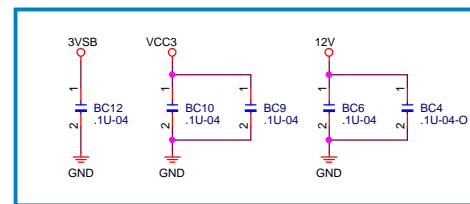
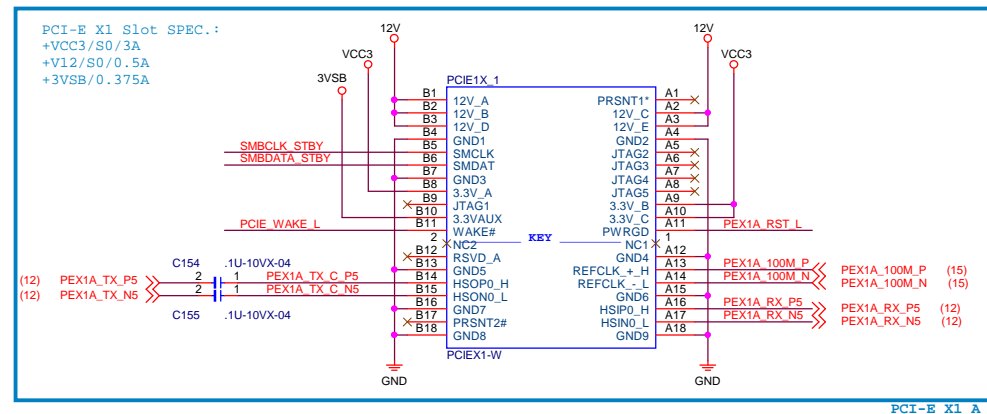
Size: Custom Document Number: **Q77H2-AD** Rev: A

Date: Monday, October 31, 2011 Sheet 15 of 49





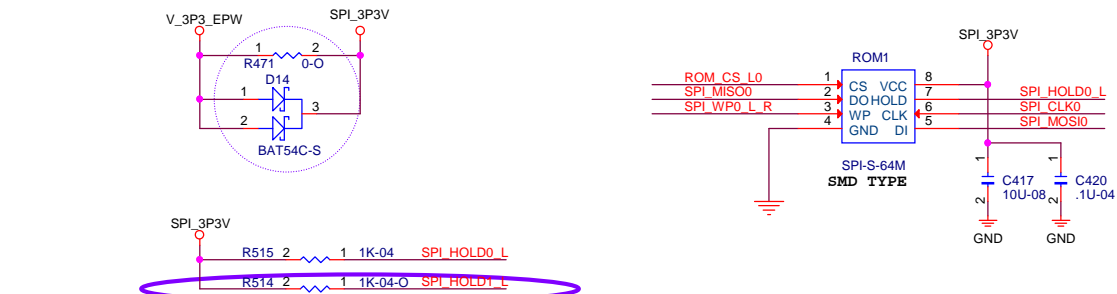
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



Elitegroup Computer Systems

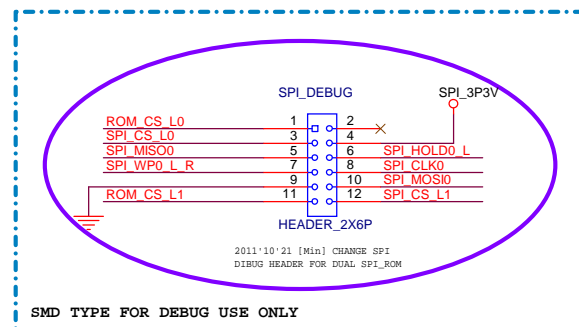
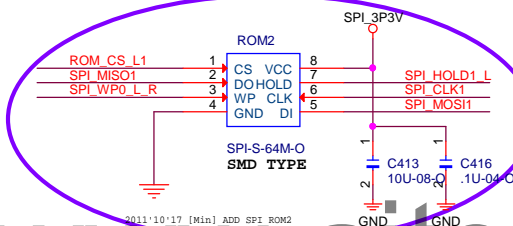
Title		Slot - PCI-EX16/PCI-EX1	Rev A
Size	Document Number	Q77H2-AD	
Custom	Monday, October 31, 2011		Sheet 20 of 49

SPI ROM Circuit

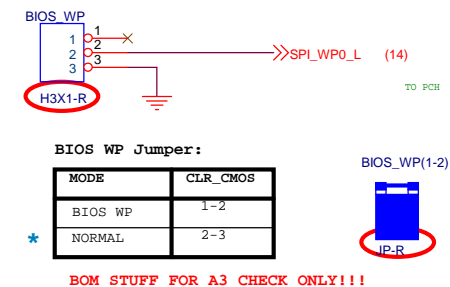


(14) SPI_MOSI >> SPI_MOSI R536 2 1 62-04 SPI_MOSI0
(14) SPI_MISO << SPI_MISO R500 2 1 62-04 SPI_MISO0
(14) SPI_CLK >> SPI_CLK R529 2 1 62-04 SPI_CLK0
(14) SPI_CS_L0 >> SPI_CS_L0 R501 1 2 0-04 ROM_CS_L0

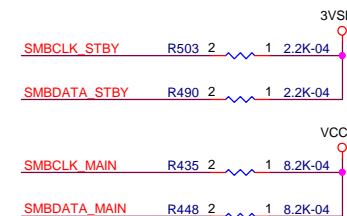
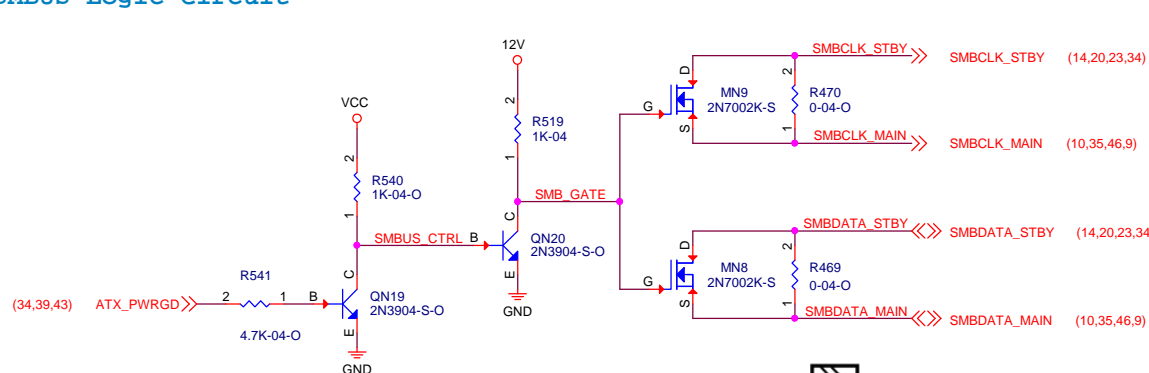
SPI_MOSI R546 2 1 62-04-O SPI_MOSI1
SPI_MISO R497 2 1 62-04-O SPI_MISO1
SPI_CLK R545 2 1 62-04-O SPI_CLK1
(14) SPI_CS_L1 >> SPI_CS_L1 R496 1 2 0-04 ROM_CS_L1

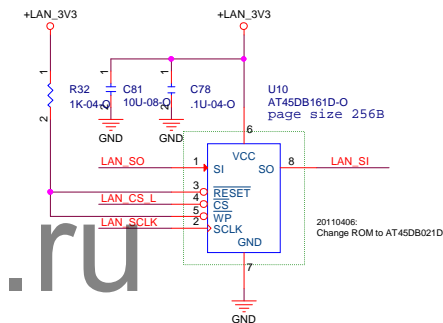
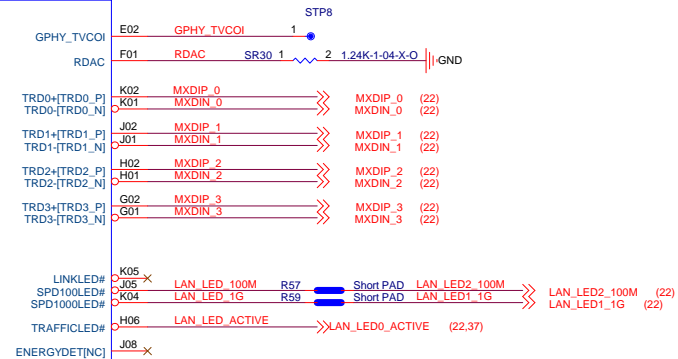
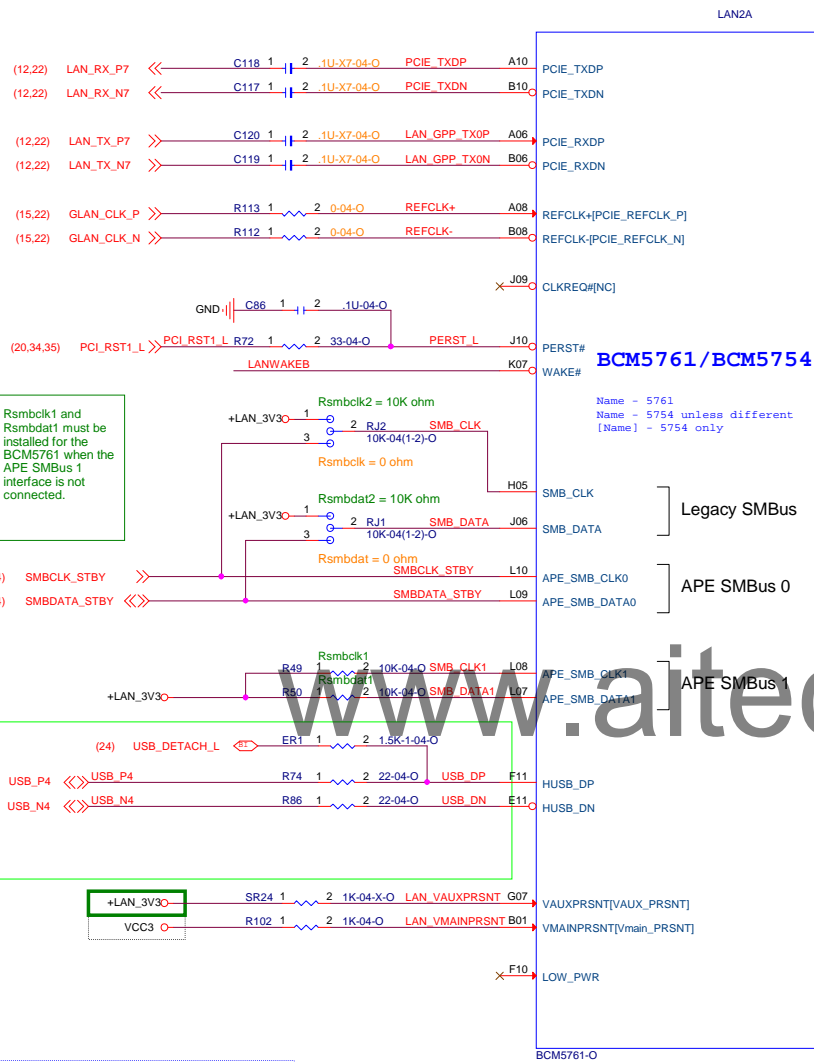


SPI_DEBUG(1-3)
MINI_JUMPER

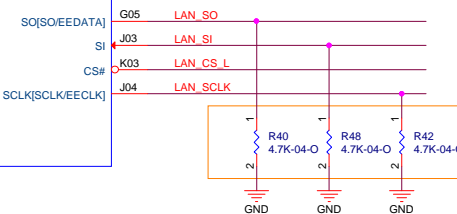


SMBUS Logic Circuit





Flash device shown is for the BCM5761 only. Refer to the BCM5754 data sheet for supported flash devices.

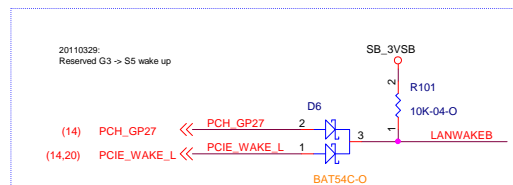


These resistors must be installed with the BCM5754 to configure flash auto-sense.

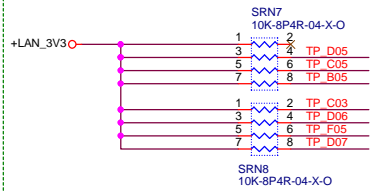
Rsmblck and Rsmdbat must be installed for the BCM5754 only.

Rsmblck1 and Rsmdbat1 must be installed for the BCM5761 when the APE SMBus 1 interface is not connected.

Rsmblck2 and Rsmdbat2 must be installed for the BCM5761 only.



These resistors must be installed with the BCM5761 only.



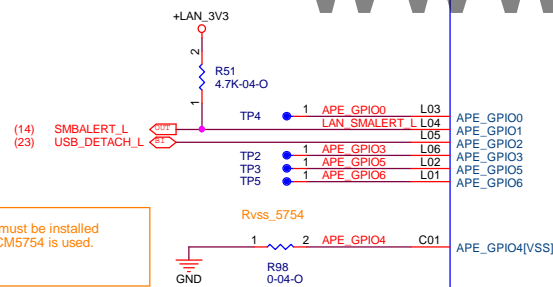
Ruart_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8_pd must be installed with the BCM5761 only.

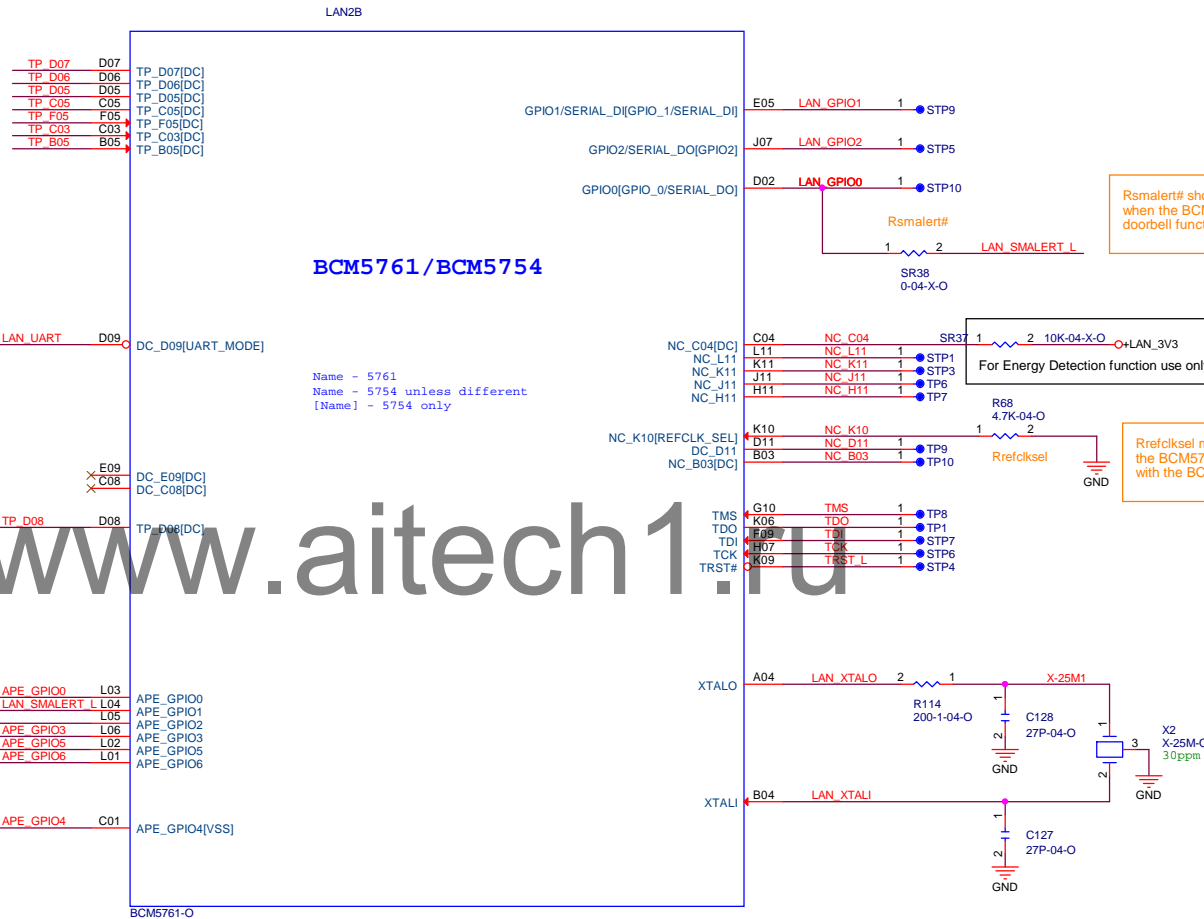


Rvss_5754 must be installed when the BCM5754 is used.



BCM5761/BCM5754

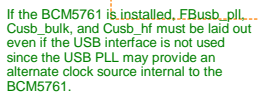
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



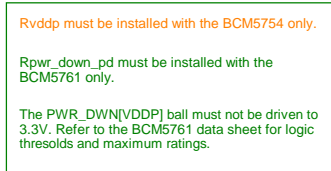
Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.

For Energy Detection function use only for 5761E use

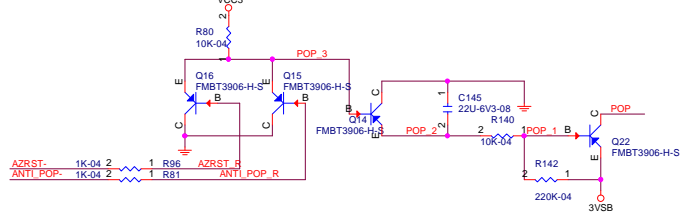
Rrefclkssel must not be installed with the BCM5761, but may be installed with the BCM5754



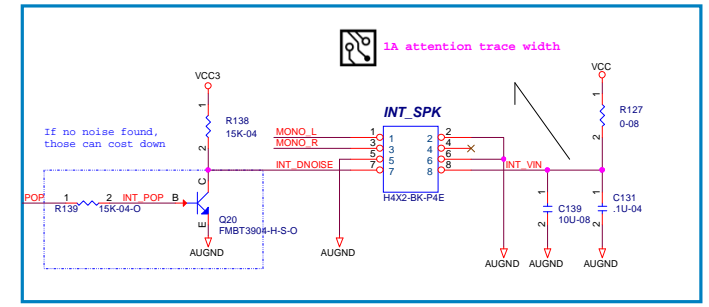
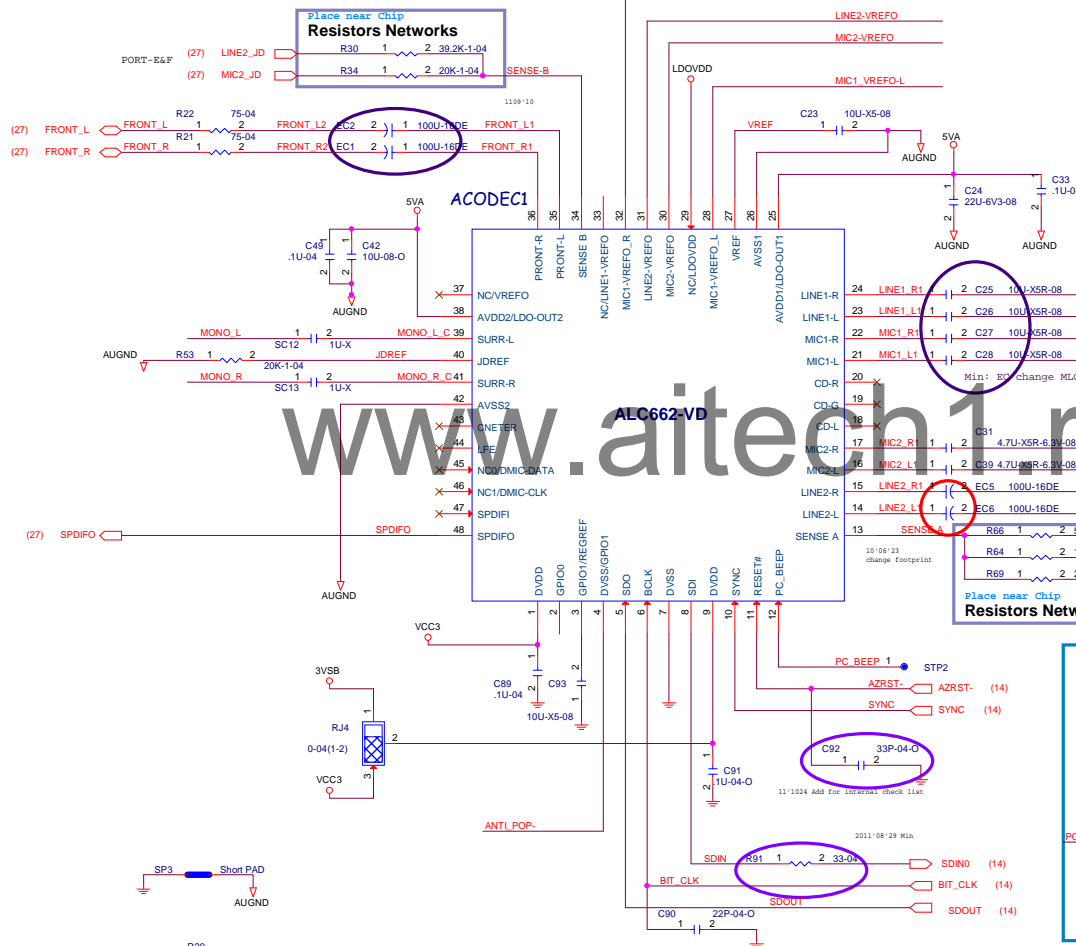
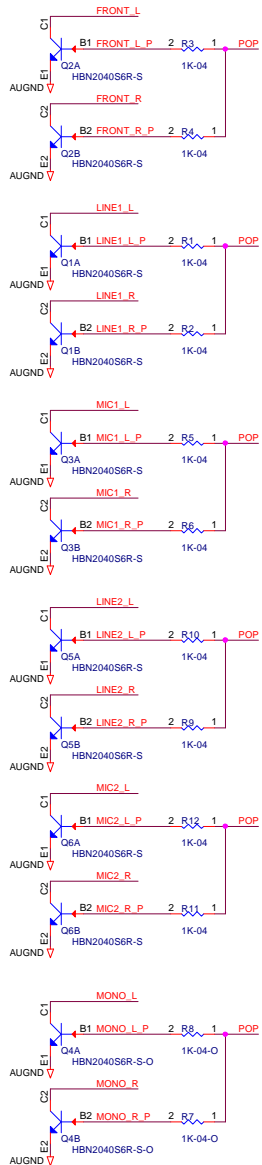
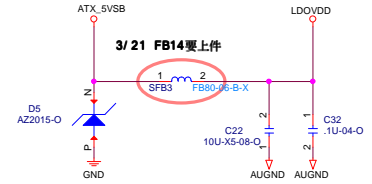
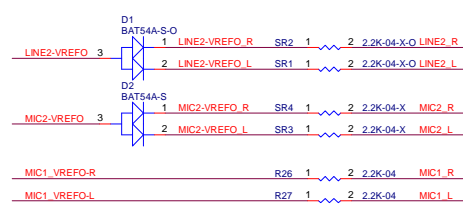
```
Name - 5761
Name - 5754 unless different
[Name] - 5754 only
```



Depop schematic

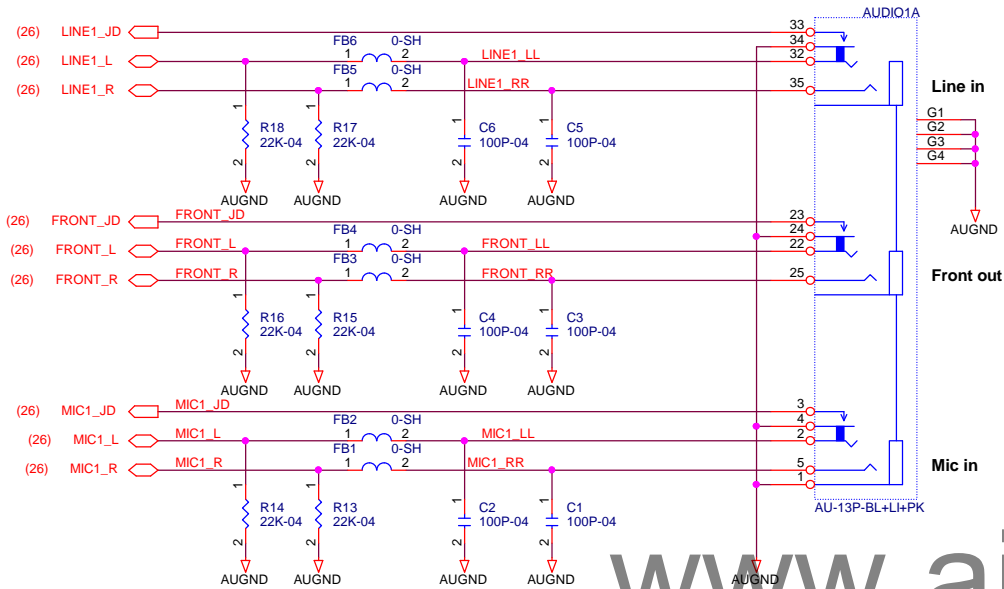


MIC Bias

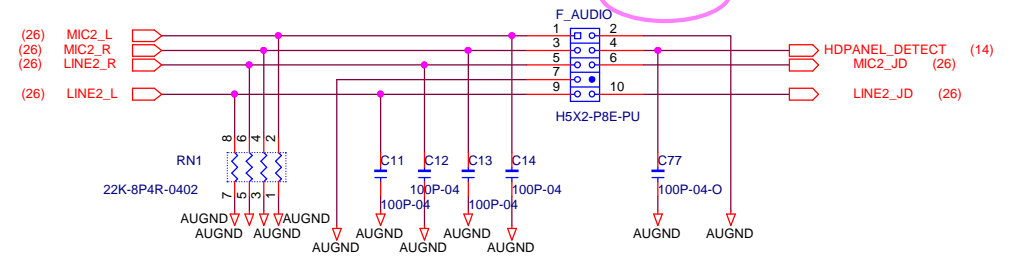


"INTERNAL SPEAKER"
FOR COMMERCIAL AND AIO SERIES USE

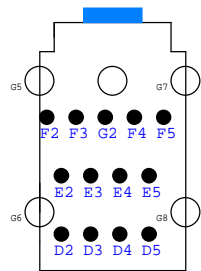
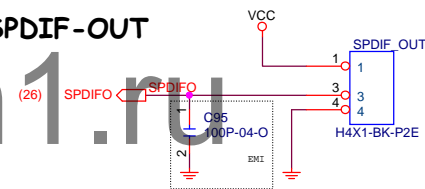
REAR-AUDIO



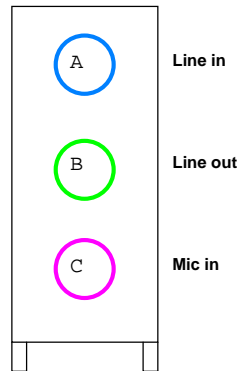
FRONT-AUDIO



SPDIF-OUT

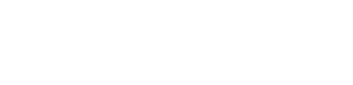
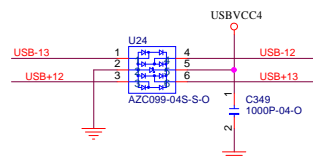
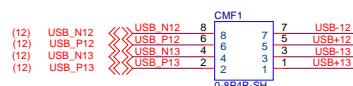
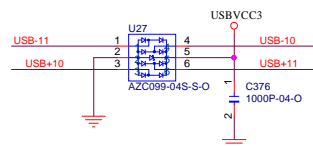
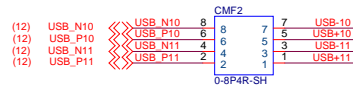
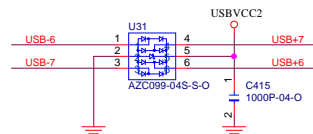
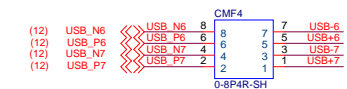


TOP VIEW



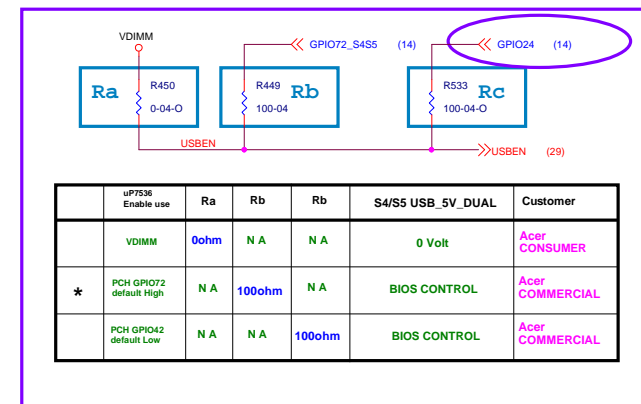
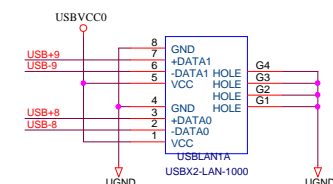
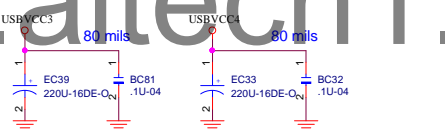
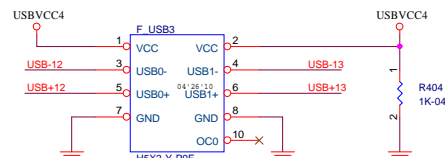
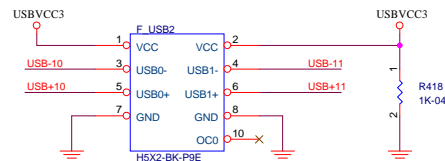
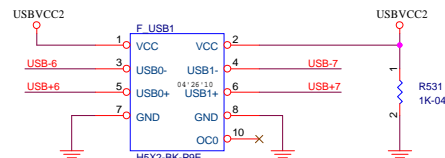
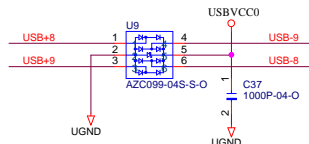
FRONT VIEW

AUDIO ALC662 Connector (PANEL)	
Size	Document Number
B	Q77H2-AD
Date:	Monday, October 31, 2011
Sheet	27 of 49

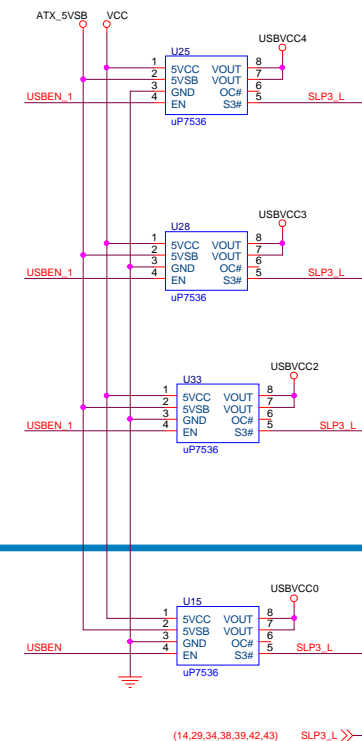


FRONT PANEL USB2.0 HEADER

REAR PANEL USB2.0 CONNECTOR



	uP7536 Enable use	Ra	Rb	Rb	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm	N A	N A	0 Volt	Acer CONSUMER
*	PCH GPIO72 default High	N A	100ohm	N A	BIOS CONTROL	Acer COMMERCIAL
	PCH GPIO42 default Low	N A	N A	100ohm	BIOS CONTROL	Acer COMMERCIAL



(12) USB_N2 <<> USB_N2
(12) USB_P2 <<> USB_P2
(12) USB_N3 <<> USB_N3
(12) USB_P3 <<> USB_P3

USB_P3 1 2 USB+3
USB_N3 3 4 USB-3
USB_P2 5 6 USB+2
USB_N2 7 8 USB-2

USB_P2 1 2 USB+2
USB_N2 3 4 USB-2
USB_P3 1 2 USB+3
USB_N3 3 4 USB-3

USB30_TX_N2_C 1 2 USB30_TX_N2_R
USB30_TX_P2_C 1 2 USB30_TX_P2_R
USB30_TX_N3_C 1 2 USB30_TX_N3_R
USB30_TX_P3_C 1 2 USB30_TX_P3_R

USB30_RX_N3 1 2 USB30_RX_N3_R
USB30_RX_P3 1 2 USB30_RX_P3_R
USB30_TX_N3_C 1 2 USB30_TX_N3_R
USB30_TX_P3_C 1 2 USB30_TX_P3_R

USB30_RX_N3 1 2 USB30_RX_N3_R
USB30_RX_P3 1 2 USB30_RX_P3_R
USB30_TX_N3_C 1 2 USB30_TX_N3_R
USB30_TX_P3_C 1 2 USB30_TX_P3_R

USB30_RX_N2 1 2 USB30_RX_N2_R
USB30_RX_P2 1 2 USB30_RX_P2_R
USB30_TX_N2_C 1 2 USB30_TX_N2_R
USB30_TX_P2_C 1 2 USB30_TX_P2_R

USB30_TX_N2_C 1 2 USB30_TX_N2_R
USB30_TX_P2_C 1 2 USB30_TX_P2_R
USB30_TX_N3_C 1 2 USB30_TX_N3_R
USB30_TX_P3_C 1 2 USB30_TX_P3_R

USB30_RX_N3 1 2 USB30_RX_N3_R
USB30_RX_P3 1 2 USB30_RX_P3_R
USB30_TX_N3_C 1 2 USB30_TX_N3_R
USB30_TX_P3_C 1 2 USB30_TX_P3_R

USB30_RX_N2 1 2 USB30_RX_N2_R
USB30_RX_P2 1 2 USB30_RX_P2_R
USB30_TX_N2_C 1 2 USB30_TX_N2_R
USB30_TX_P2_C 1 2 USB30_TX_P2_R

USB_N0 1 2 USB-0
USB_P0 3 4 USB+0
USB_N1 5 6 USB-1
USB_P1 7 8 USB+1

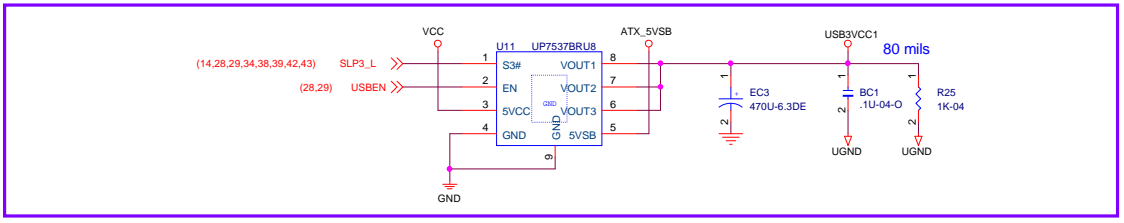
USB30_TX_N0 1 2 USB30_TX_N0_C
USB30_TX_P0 1 2 USB30_TX_P0_C
USB30_RX_N0 1 2 USB30_RX_N0_R
USB30_RX_P0 1 2 USB30_RX_P0_R

USB30_RX_N0 1 2 USB30_RX_N0_R
USB30_RX_P0 1 2 USB30_RX_P0_R
USB30_TX_N1 1 2 USB30_TX_N1_C
USB30_TX_P1 1 2 USB30_TX_P1_C

USB30_RX_N1 1 2 USB30_RX_N1_R
USB30_RX_P1 1 2 USB30_RX_P1_R
USB30_TX_N1_C 1 2 USB30_TX_N1_R
USB30_TX_P1_C 1 2 USB30_TX_P1_R

USB30_TX_P1_R 1 2 USB30_TX_P1_R
USB30_TX_N1_R 1 2 USB30_TX_N1_R
USB30_TX_P0_R 1 2 USB30_TX_P0_R
USB30_TX_N0_R 1 2 USB30_TX_N0_R

USB30_RX_N0_R 1 2 USB30_RX_N0_R
USB30_RX_P0_R 1 2 USB30_RX_P0_R
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USB30_RX_P1_R 1 2 USB30_RX_P1_R



USB3 ESD COMPONENTS

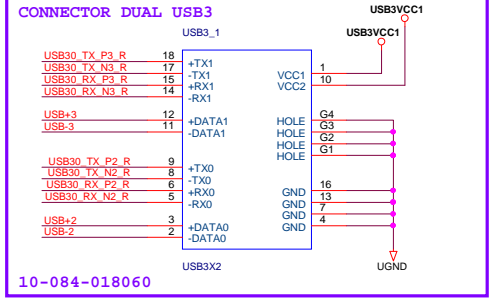
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USB30_TX_P2_R 1 2 USB30_TX_P2_R
USB30_TX_N3_R 1 2 USB30_TX_N3_R
USB30_TX_P3_R 1 2 USB30_TX_P3_R

USB30_RX_N3_R 1 2 USB30_RX_N3_R
USB30_RX_P3_R 1 2 USB30_RX_P3_R
USB30_RX_N2_R 1 2 USB30_RX_N2_R
USB30_RX_P2_R 1 2 USB30_RX_P2_R

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USB30_TX_P3_R 1 2 USB30_TX_P3_R
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USB30_RX_P3_R 1 2 USB30_RX_P3_R

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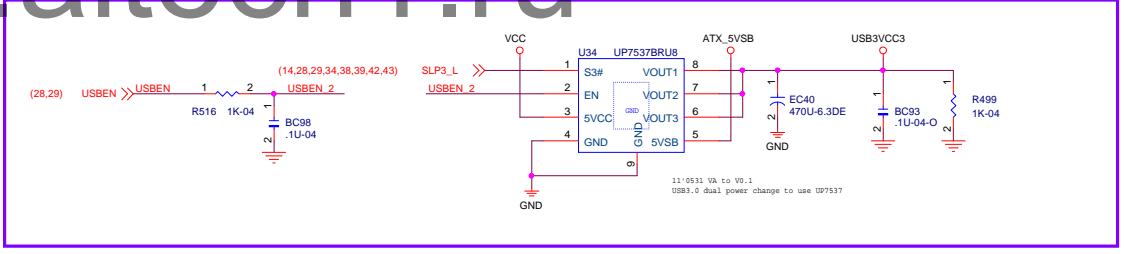
NOTE: Port1,Port2 SWAP between Port3, Port4
2011'03'11



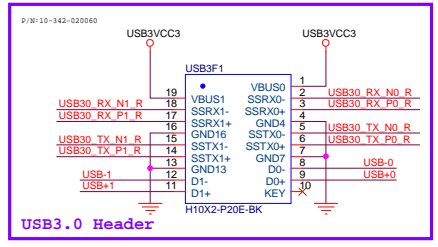
REAR PANEL USB3.0 CONNECTOR

FRONT PANEL USB3.0 HEADER

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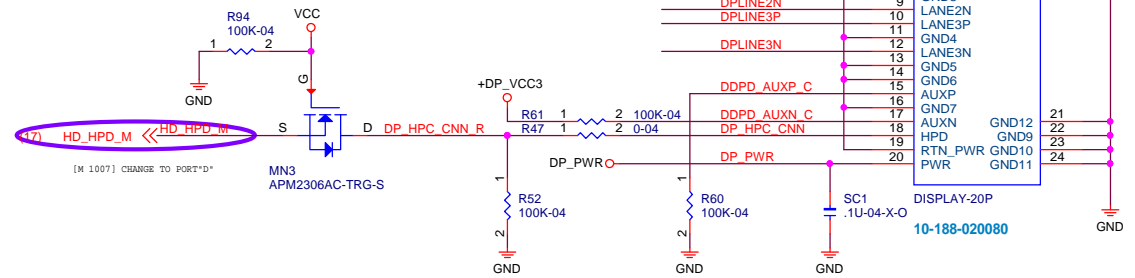
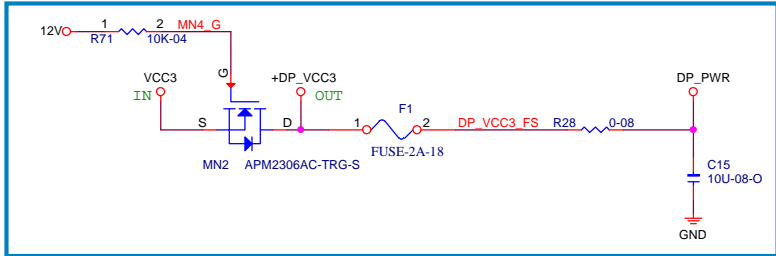
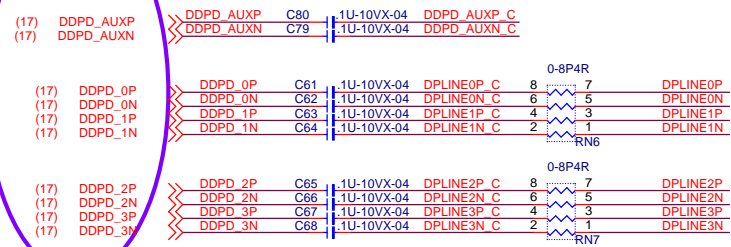


USB3 ESD COMPONENTS



USB3.0 Header

[M 1007] CHANGE TO PORT"D"

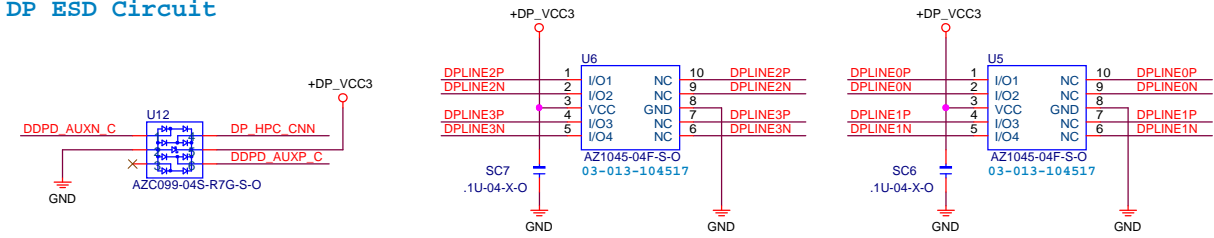


www.aitech1.ru

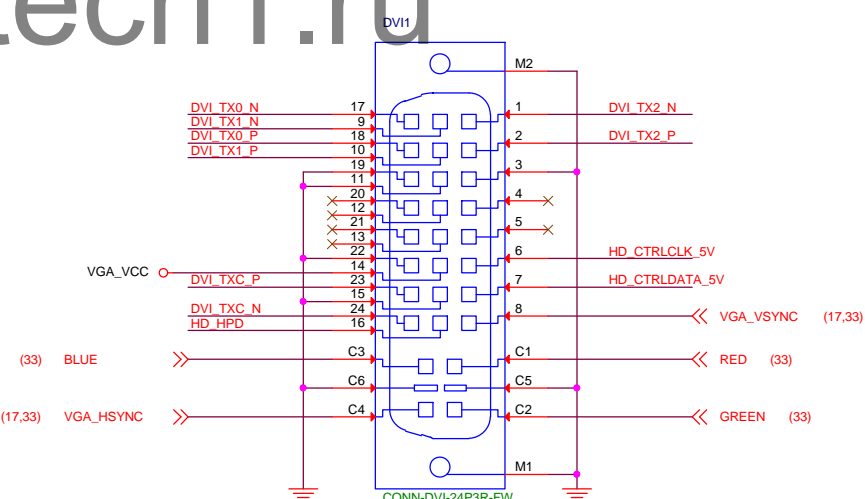
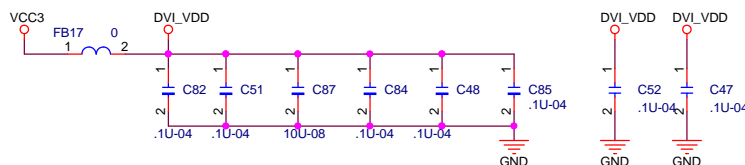
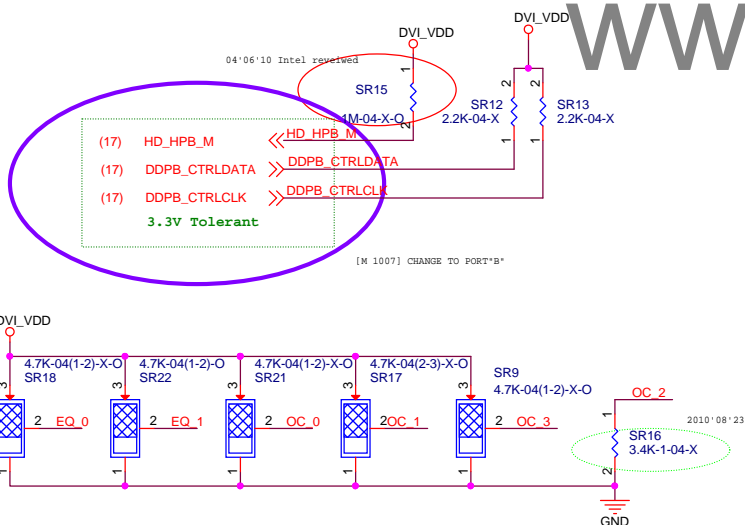
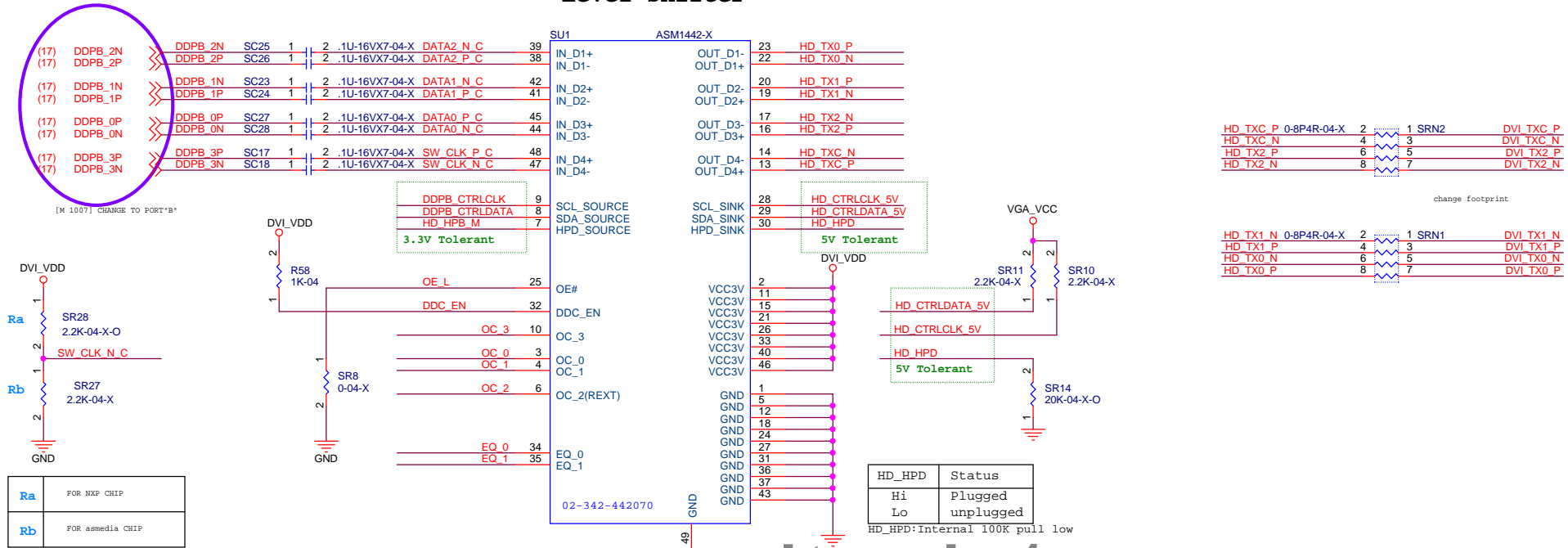
2011'10'17 [Min] DEL DP Port2 support HDMI DONGLE

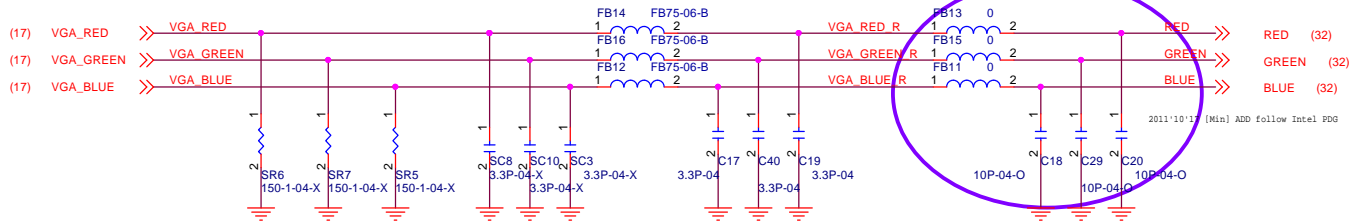
SUPPORT DP TO HDMI/DVI DONGLE

DP ESD Circuit

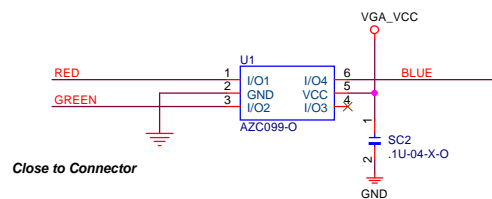
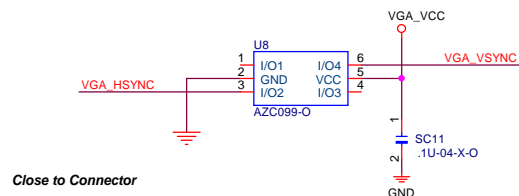
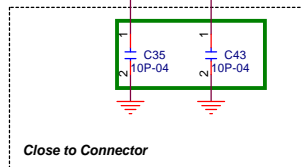
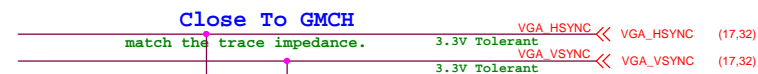


Level Shifter



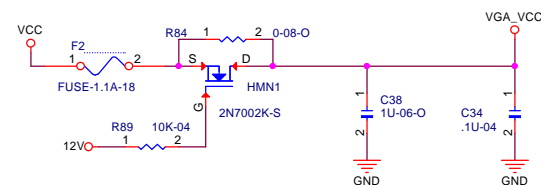


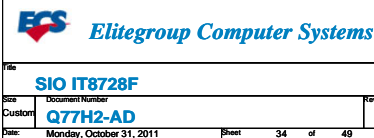
Close to Connector

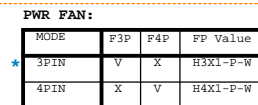
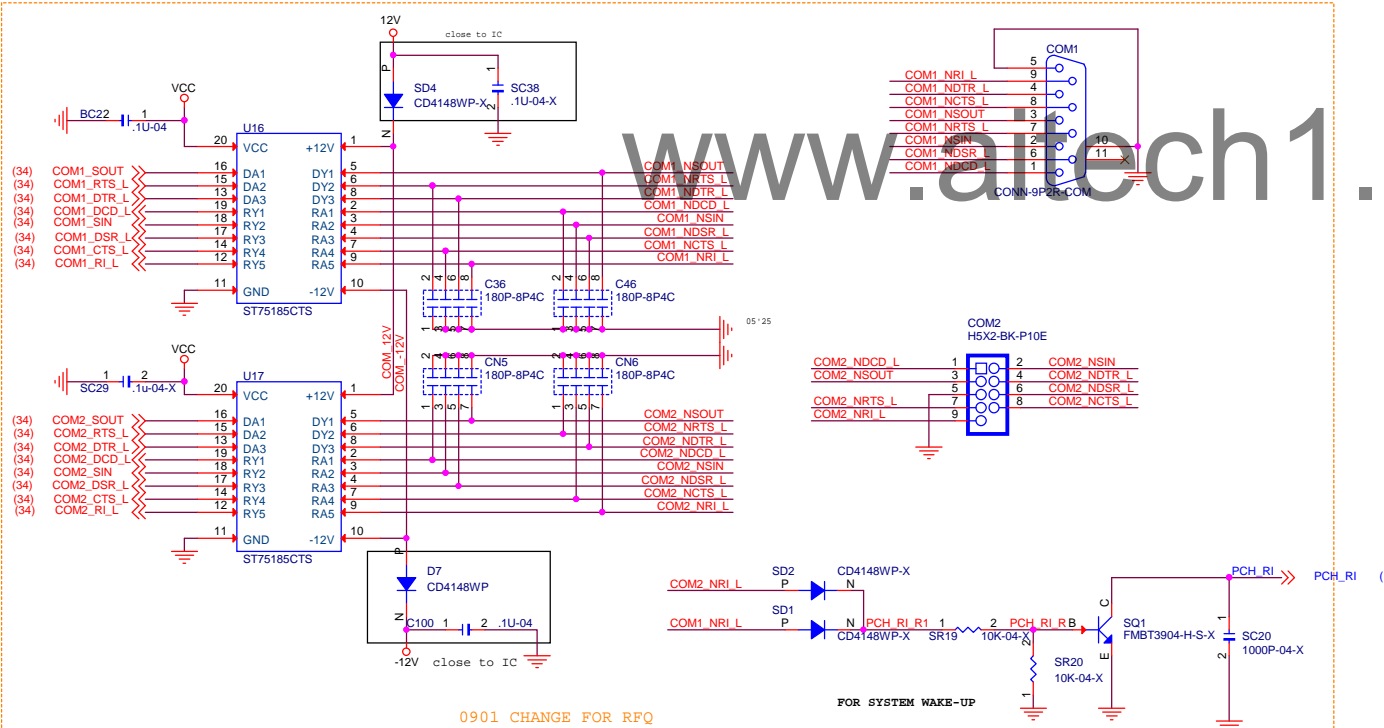


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If build in Internal DVI/HDMI Con,
that can use the circuit to protect reverse voltage together.



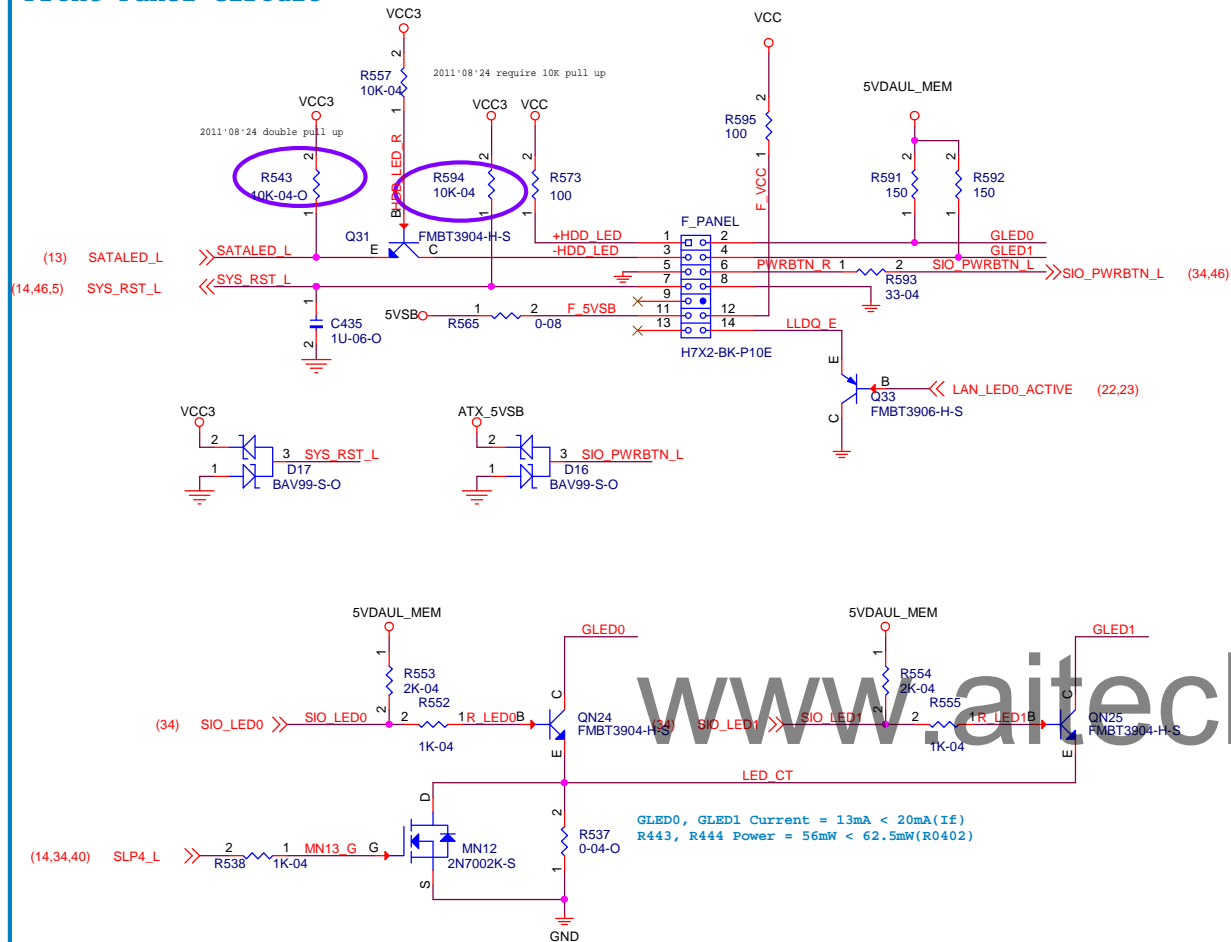




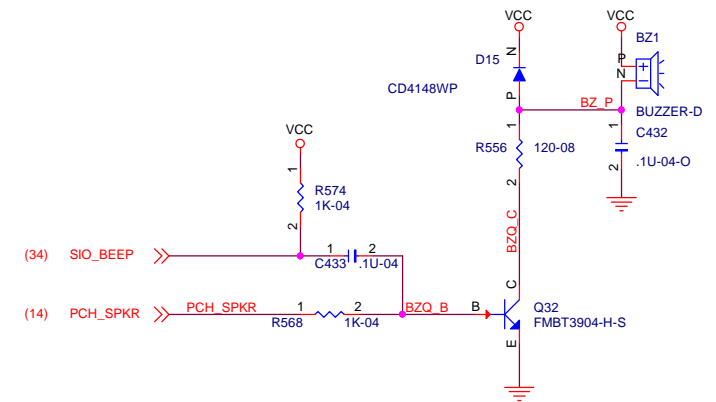
0901 CHANGE FOR RFQ

+ - terminal add short pad to ground for nonuse OP , 20110406

Front Panel Circuit



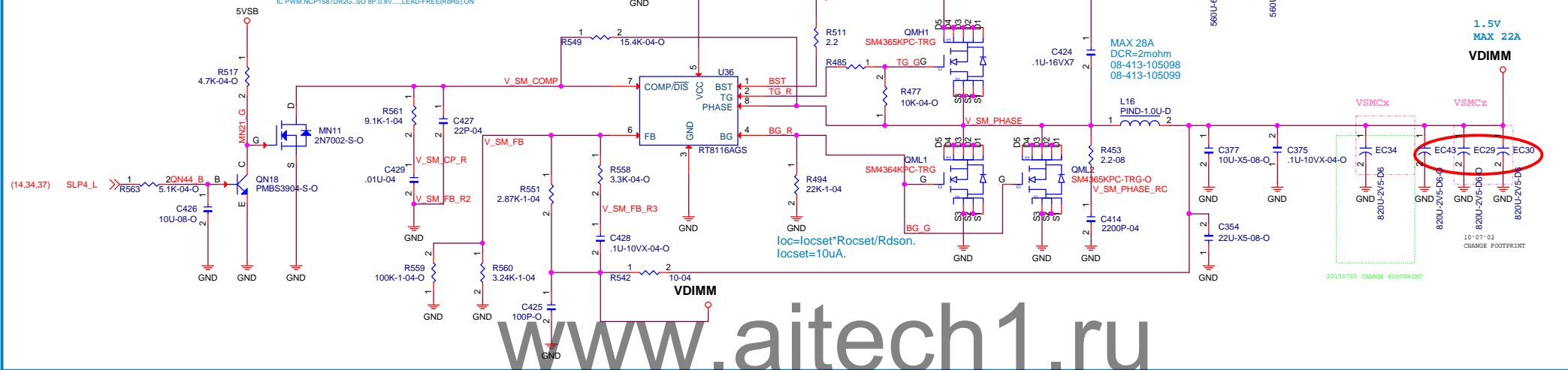
Buzzer Circuit



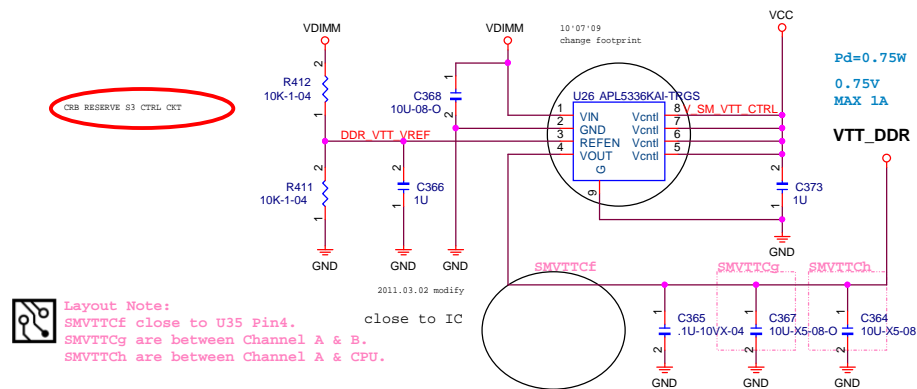
SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.

02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON



AP5336/GS9020/AME9172M



VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



- I_{SS} is the soft-start current source at the 20 μ A limit
- V_{SRFF} is the buffered V_{RFF} reference voltage

TABLE 2. ISL95870B VID TRUTH TABLE

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (EQ. 21)$$

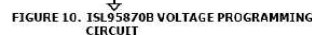
The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (EQ. 22)$$

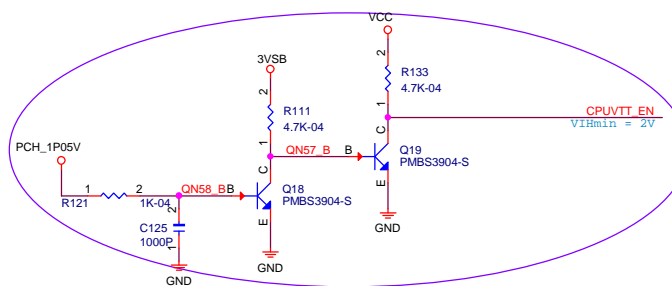
The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET2} + R_{SET4}} \right) \quad (\text{EQ. 23})$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (EQ. 24)$$


Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC



★

Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



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change to 4.7K for BAD Power Supply.

ATX_PW-24P2R

ATX_PSON L

ATX_PSON L (34)

C389 470P-04

GND

ATX_PWRGD (21,34,39)

BC87 .1U-04

GND

BC88 .1U-04

GND

R431 4.7K-04

R432 10K-04

Reserve for +5VSB G3 Discharge.

OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5 (CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

PWR CONN CAPS

ATX_5VSB

BC89 .1U-04-0

GND

VCC

BC90 .1U-04-0

GND

VCC3

C387 .1U-04-0

GND

BC65 .1U-04-0

GND

12V

BC91 .1U-04-0

GND

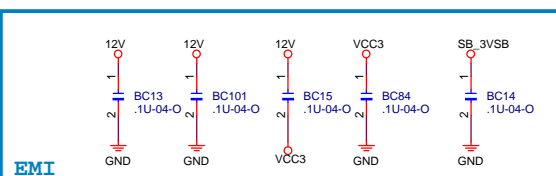
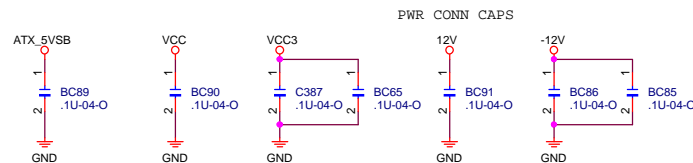
-12V

BC86 .1U-04-0

BC85 .1U-04-0

GND

OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



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CSA Sequence

The diagram illustrates the CSA Sequence circuit, featuring two comparators, QN13 and QN14, both of type PMBS3904-S. The circuit is powered by a 5VSB supply and includes a 0-04-O output.

Comparator QN13 (PMBS3904-S):

- Input 1:** QN3_B (10K-04)
- Input 2:** VTT_PWRGD (41)
- Output:** QN13_B

Comparator QN14 (PMBS3904-S):

- Input 1:** QN8_B (10K-04)
- Input 2:** SLP3_L ((14,28,29,34,38,39,42))
- Output:** QN14_B

Other Components:

- Resistors:** R466, R484, R521, R522, R523.
- Transistors:** QN10, QN11 (PMBS3904-S).
- Power Supply:** 5VSB.
- Ground:** GND.
- Output:** 0-04-O.

